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# Analysis of the Best Topology is Investigated in MLI

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**ABSTRACT:** This paper is about multilevel inverter (MLI) with various topologies. The motivation behind paper incorporates understanding and analyzing the performance of three unique topologies of multilevel inverter which are Diode Clamped Multilevel Inverter (DCMI), Flying Capacitor Multilevel Inverter (FCMI) and Cascaded H-connect Multilevel Inverter (CHMI). The Cascaded H bridge multilevel inverter is considered as the proposed topology to be utilized in this paper. The correlations are finished as for losses, cost, weight and THD. This assessment is help to which kind of MLI is ideal. The normal that the plan of the CHB inverter to Produce output voltage waveform of the Multilevel Inverter (MLI) with less harmonic distortion compared with the two-level inverter, Produce almost sinusoidal waveform without using any filter circuit, Produce better yield voltages when using particle swarm optimization (PSO) algorithm.

**KEYWORDS:** Multilevel Inverter, Different topologies (FC-MLI, DC-MLI, CHB-MLI), Total harmonic distortion (THD), Particle Swarm Optimization (PSO) algorithm.

## I. INTRODUCTION

Recently, electric energy usage is expanding quickly because of the expanding of the energy demand on the globe. One of the most important advances in power electronics is multilevel inverter. Generally used technique is CHB. The most important three MLI configurations are neutral point converter, flying capacitor and cascaded H-bridge multilevel inverter are investigated and choosing the best inverter [1, 2]. The diode clamped inverter in a five- level inverter [3, 4, 5, and 6] and flying capacitor is explored in the various papers [7, 8, and 9]. numerous different methods additionally exist [10]. Specifically, among these techniques, CHB single-phase inverters have drawn consideration due to their modularized circuit design and simplicity. An assortment of modulation techniques can be applied to CHB inverters. To additionaly add more CHBs, the number of output levels inverters increments.Generally, if the quantity of output voltage levels is improved, then the number of power electronic devices and the number of isolated DC sources is also increased. This creates a CHB inverter more difficult; the number of power electronics switches is very high. The reason for this investigation is to build the voltage level to accomplish sinusoidal waveform with less number of switches. Think about various voltage levels by expanding the levels with less harmonic distortion by make use of particle swarm optimization algorithm.

## II.PROBLEM STATEMENT

In the traditional topologies having more switching devices are used to design a multilevel inverter circuit and generate the less number of output level is presented. As a result of conventional topologies having more harmonics, less efficiency, switching losses will be high and also THD is high. These harmonics can't reduce easily. So presented and build a new multilevel inverter.

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## III.TOPOLOGIES OF MLI

The multilevel inverters contain a group of power switching devices and voltage sources. Since it is fit to make yield voltage waveforms with a better harmonic range and achieve higher voltages levels with a limited switching device.

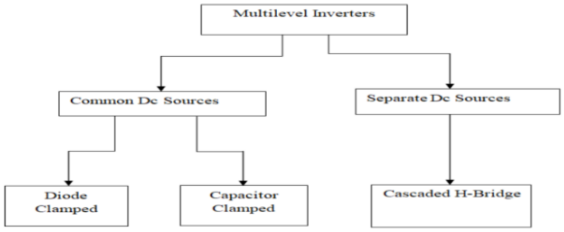


Figure.1. Topology for multilevel inverter

The category of multilevel inverter topologies is exposed in certain below figure 1. There are three major categories they are diode-clamped (neutral-clamped), capacitor clamped (flying capacitors), and cascaded H bridge inverter.

### A.DIODE CLAMPED MULTILEVEL INVERTER

The primary idea of this inverter is to use diodes to limit the power electronics devices voltage stress. The voltage over every capacitor and each switch is $V_{dc}$. 5-level diode clamped multilevel inverter appears in figure 2a. Diode clamped multilevel inverter is also called as neutral-point clamped (NPC-MLI) inverter. In a 5-level diode clamped inverter, to calculate the number of switches, diodes and capacitors are using formulas.

For five-level inverter m=5, the Number of switches is 2(m-1) =8, Number of diodes is (m-1) (m-2) =12, Number of capacitors is (m-1) =4.

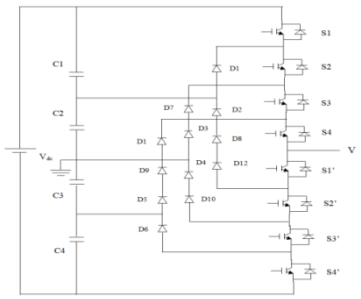


Figure 2.a A 5 level DC-MLI

As it tends to be seen in Table.1 the greatest yield voltage it is half of the DC source. It is a disadvantage of the diode clamped multilevel inverter. This issue can be made clear by using a two times voltage source or cascading two diode clamped multilevel inverters. The switching angles must be determined so that the THD of the output voltage becomes as low as could be expected under the conditions. In this approach, the lower order harmonics can be reduced by select considered switching angles. An m level inverter needs (m-1) voltage sources, 2(m-1) switching devices and (m-1) (m-2) diodes.

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| Vout | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_1$' | $S_2$' | $S_3$' | $S_4$' |
|---|---|---|---|---|---|---|---|---|
| $V_{dc}$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $3V_{dc}/4$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| $V_{dc}/2$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $V_{dc}/4$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

Table.1. Switching pattern for diode clamped MLI

In this method, the lower order harmonics can be eliminated by choosing calculated switching angles. In case to have $V_{dc}$ is the output, the switches S1 to S4 should conduct simultaneously. For every voltage levels four switches should perform.

### B.FLYING CAPACITOR MULTILEVEL INVERTERS

Flying capacitor multilevel inverter is also called as capacitor clamped (CC-MLI) inverter. This inverter employs capacitors to limit the voltage of the power electronic devices. The design of the flying capacitor multilevel inverter resembles a diode clamped multilevel inverter except that capacitors are utilized to separate the input DC voltage. The voltage over every capacitor and each switch is $V_{dc}$. Five- level flying capacitor multilevel inverter has appeared in figure 2b. For a 5-level flying capacitor multilevel inverter, m=5. The Number of switches is 2(m-1) =8, Number of capacitors is (m-1) (m-2)/2=6. This strategy is equivalent to the diode clamped inverter.

The switching conditions of this inverter are resembled in the diode clamped multilevel inverter. It implies that for each yield voltage level 4 switches should be on. Table.2 shows the switching condition for a 5-level flying capacitor clamped multilevel inverter.

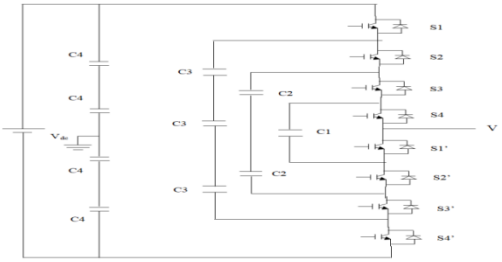


Figure 2.b A 5 level FC-MLI

Five- level flying capacitor multilevel inverter has appeared in figure 2b. There are 8 switches are used.

| Vout | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_4$' | $S_3$' | $S_2$' | $S_1$' |
|---|---|---|---|---|---|---|---|---|
| $V_{dc}$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $3V_{dc}/4$ | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| $V_{dc}/2$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $V_{dc}/4$ | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

Table2. Switching pattern for capacitor clamped MLI

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The switching angles similar to the diode clamped multilevel inverter supposed to be calculated in such a way that the THD of the output voltage becomes as low as possible. An m level inverter needs (m-1) voltage sources, 2(m-1) switching devices, (m-1) (m-2)/2 clamping capacitor.

### C.CASCADED H-BRIDGE MULTILEVEL INVERTER

Figure. 2c shows a five-level cascaded H-bridge multilevel inverter. This inverter contains the two H bridge inverters that are coupled in cascade.

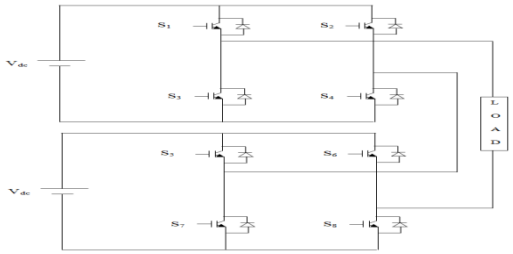


Figure 2.c A 5 level CHB-MLI

For a 5-level cascaded H-bridge multilevel inverter having 8 switches is required. The idea of this inverter is to interfacing H-connect inverters in series to get a sinusoidal output voltage. The number of yield voltage level is 2m+1, where m is the number of cells.

| Vo | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ |
|---|---|---|---|---|---|---|---|---|
| $V_{dc}/2$ | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $-V_{dc}/2$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| $-V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

Table.3. a switching pattern for cascaded H-bridge MLI.

A multilevel inverter can be consist of a power electronics device that can generate a staircase waveform. In five-level outputs are $V_{dc}$, $2V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$ is shown in the below diagram. It produces the generalized stepped waveform is also shown below in figure3.

| MLI Topology | DCMLI | FCMLI | `CMLI |
|---|---|---|---|
| Power semiconductor switches | 2(m-1) | 2(m-1) | 2(m-1) |
| Clamping Diodes | (m-1)(m-2) | - | - |
| Clamping Capacitors | - | (m-1)(m-2)/2 | - |
| DC Bus capacitors | (m-1) | (m-1) | (m-1)/2 |
| %THD level | High | Average | small |
| Output Voltage levels | 5 | 5 | 5 |

Table.4. Comparison of the multilevel inverter topology

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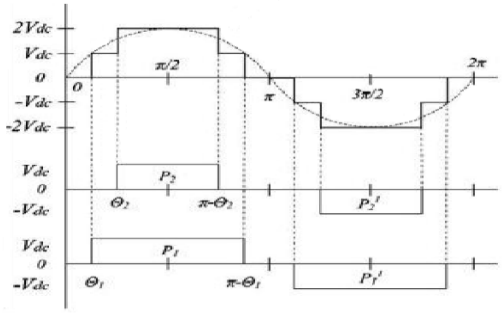


Figure.3. Five level output waveform

An m level cascaded H-bridge inverter requires 2(m-1) switching device where m is the number of the output voltage level. Each level of the full-bridge converter comprises four switches. For instance, by turning ON S1 and S4, yield +Vdc, Turing ON S2 and S3, yields -Vdc. Turning OFF all switches yields Vdc=0.

## IV.MATLAB MODEL AND RESULT

In the result for the five level diode clamped, clamping capacitor and cascaded inverter is shown in given below figure. The result and FFT analysis for diode clamped inverter is shown in figure 4 and 5.

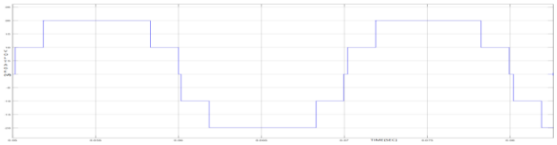

Figure.4. Five level output waveform for DC-MLI

The MALTAB simulation result for five-level diode clamped multilevel inverter is shown in above diagram. The output voltage is shown in figure 4.

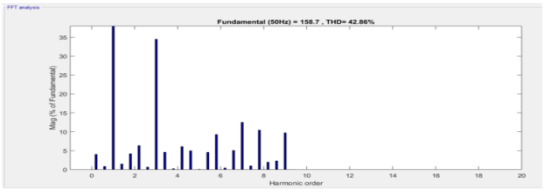

Figure.5. FFT analysis of diode clamped inverter

The result and FFT analysis for diode clamped inverter is shown figure 5. The harmonic level is 42.86%.

Figure.6. Five level output waveform for FC-MLI

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Figure.6. Shown in the output voltage for using MALTAB simulation result for five-level clamping capacitor is shown in above diagram.

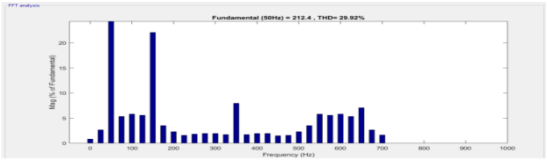

Figure.7. FFT analysis of clamping capacitor inverter

FFT analysis of output voltage for FC-MLI is shown in the figure 7. The harmonic level is 29.92%. The clamping capacitor is having less harmonic with compared to the diode clamped inverter.

The MATLAB simulation model for two cascaded H bridge inverter is connected in parallel it is shown in below figure 8.

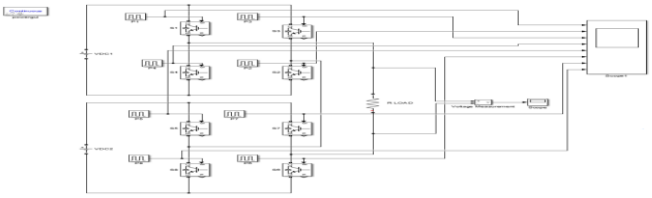

Figure.8. MATLAB model for CHB-MLI

The result and FFT analysis for clamping capacitor inverter is shown in the figure 9 and 10. The percentage of the THD for diode clamped, flying capacitor and cascaded inverter of five-level is shown in the figure 5, 7, and 10. The comparison for different topology of multilevel inverter is shown in below table 5.

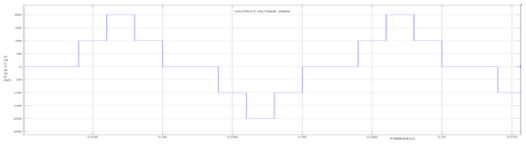

Figure.9. Five level output waveform for CHB-MLI

Figure.9. Shown in the output voltage for using MALTAB simulation result for five-level cascaded h bridge inverter is shown in above diagram.

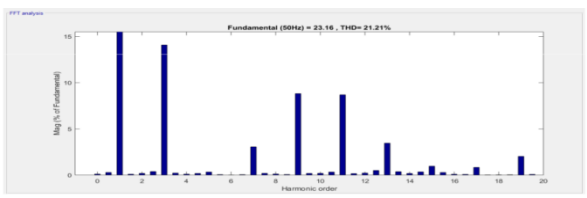

Figure.10.FFT analysis of diode clamped inverter

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FFT analysis of output voltage for CHB-MLI is shown in the figure 7. The harmonic level is 21.21%. The CHB inverter is having less harmonic with compared to the diode clamped and clamping capacitor inverter.

| m-Level Multilevel Inverter | Harmonic Content (%) | | |
|---|---|---|---|
| | Diode Clamped | Capacitor Clamped | Cascaded H- Bridge |
| Five-level | 42.86% | 29.92% | 21.2% |

Table.5. Percentage of THD is Compare with different topologies of multilevel inverter.

From this analysis the cascaded H bridge inverter produced less THD with less power electronic switching devices. In this CHB-MLI helps to produce the output for near sinusoidal with minimum switching device and harmonic distortion.

## V.CONCLUSION

This paper described multilevel inverter (MLI) with different topologies. The decision of this various topology for founded on which inverter is used. This paper joins analyze the performance of three types of topologies of multilevel inverter which are Diode Clamped Multilevel Inverter (DCMI), Flying Capacitor Multilevel Inverter (FCMI) and Cascaded H-bridge Multilevel Inverter (CHMI). The cascaded H-bridge multilevel inverter setup is utilized for producing better output. This configuration contains less number of switches and produce lesser harmonics in the output voltage. The H-bridge inverter is better than the diode clamped multilevel inverter and flying capacitor inverter as it comprises of less component, diodes and capacitors are absent in the cascaded H-bridge inverter.

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